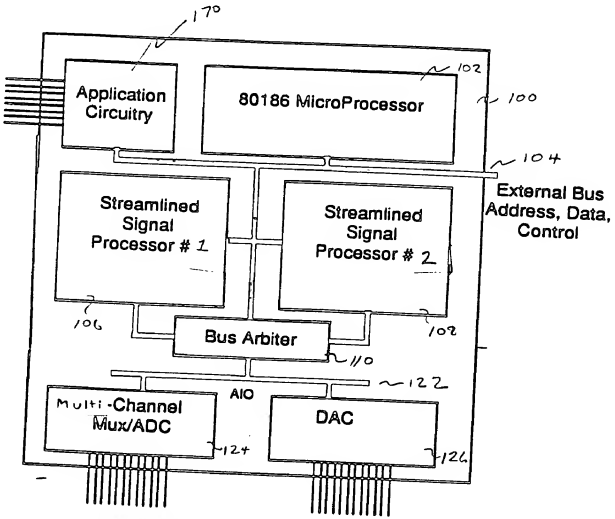
170
Application Circuitry
80186 MicroProcessor
102
100
104
External Bus Address, Data, Control
Streamlined Signal Processor # 1
Streamlined Signal Processor # 2
106
Bus Arbiter
102
110
122
AIO
Multi-Channel Mux/ADC
124
DAC
126

FIGURE 1a

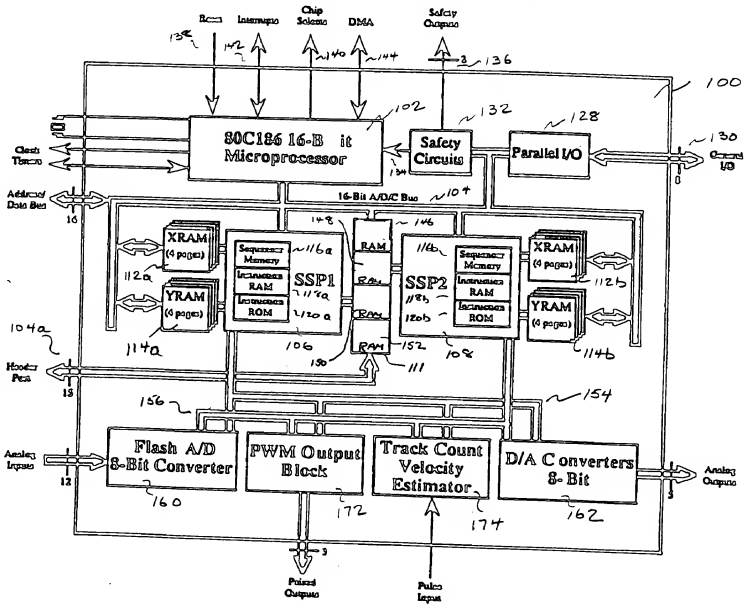
Resets
Interrupts
Chip Selects
DMA
Safety Outputs
138
142
140
144
136
100
102
132
128
130
80C186 16-Bit Microprocessor
Safety Circuits
Parallel I/O
Clock Timers
Address/ Data Bus
16
134
16-Bit A/D/C Bus
104
148
146
XRAM (4 pages)
YRAM (4 pages)
112a
114a
Sequence Memory
Instruction RAM
Instruction ROM
SSP1
116a
118a
120a
106
RAM
150
152
111
SSP2
116b
118b
120b
108
112b
114b
104a
Header Pins
15
156
154
Analog Inputs
12
Flash A/D 8-Bit Converter
160
PWM Output Block
172
Track Count Velocity Estimator
174
D/A Converters 8-Bit
162
Analog Outputs
3
Pulsed Outputs
Pulse Inputs

FIGURE 1b

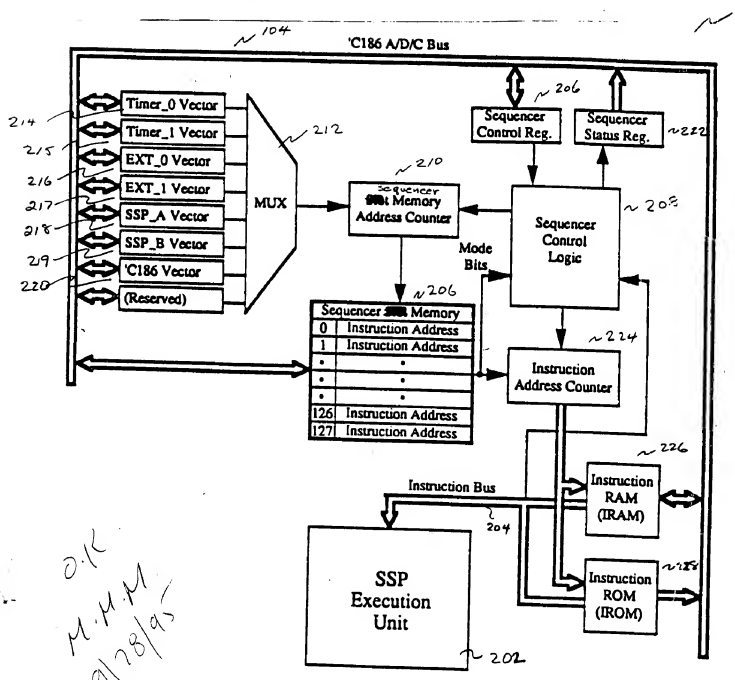
200
104
'C186 A/D/C Bus
206
Sequencer Control Reg.
Sequencer Status Reg.
222
214
Timer_0 Vector
215
Timer_1 Vector
216
EXT_0 Vector
217
EXT_1 Vector
218
SSP_A Vector
219
SSP_B Vector
220
'C186 Vector
(Reserved)
212
MUX
210
Sequencer Memory Address Counter
208
Sequencer Control Logic
Mode Bits
206
Sequencer Memory
0 Instruction Address
1 Instruction Address
126 Instruction Address
127 Instruction Address
224
Instruction Address Counter
226
Instruction RAM (IRAM)
Instruction Bus
204
228
Instruction ROM (IROM)
SSP Execution Unit
202

FIGURE 2

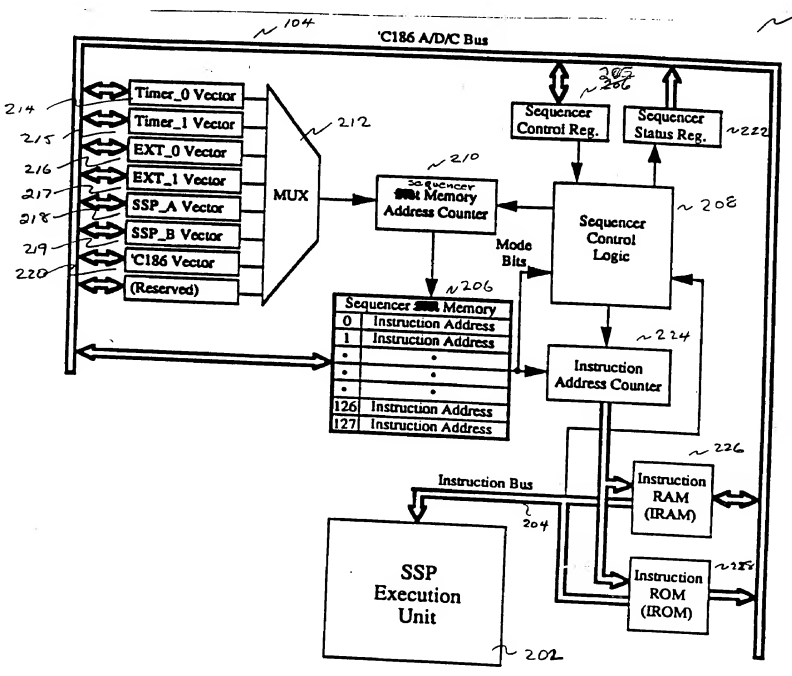
200
104
'C186 A/D/C Bus
214
215
216
217
218
219
220
Timer_0 Vector
Timer_1 Vector
EXT_0 Vector
EXT_1 Vector
SSP_A Vector
SSP_B Vector
'C186 Vector
(Reserved)
MUX
212
Sequencer Control Reg.
Sequencer Status Reg.
222
210
Sequencer Next Memory Address Counter
Sequencer Control Logic
208
Mode Bits
206
Sequencer Next Memory
0 Instruction Address
1 Instruction Address
126 Instruction Address
127 Instruction Address
224
Instruction Address Counter
226
Instruction Bus
204
Instruction RAM (IRAM)
228
Instruction ROM (IROM)
SSP Execution Unit
202

FIGURE 2

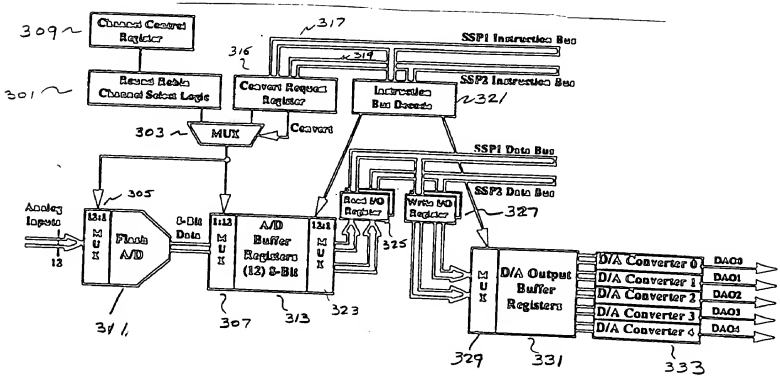
309
Channel Control Register
317
SSP1 Instruction Bus
316
314
301
Read Table Channel Select Logic
Convert Request Register
Instruction Bus Decode
SSP2 Instruction Bus
321
303
MUX
Convert
SSP1 Data Bus
SSP2 Data Bus
305
Read I/O Register
Write I/O Register
327
Analog Inputs
13:1
MUX
Flash A/D
12
0-Bit Data
11:3
A/D Buffer Registers (12) 8-Bit
12:1
MUX
325
D/A Output Buffer Registers
D/A Converter 0
D/A Converter 1
D/A Converter 2
D/A Converter 3
D/A Converter 4
DAO0
DAO1
DAO2
DAO3
DAO4
311
307
313
323
329
331
333

FIGURE 3

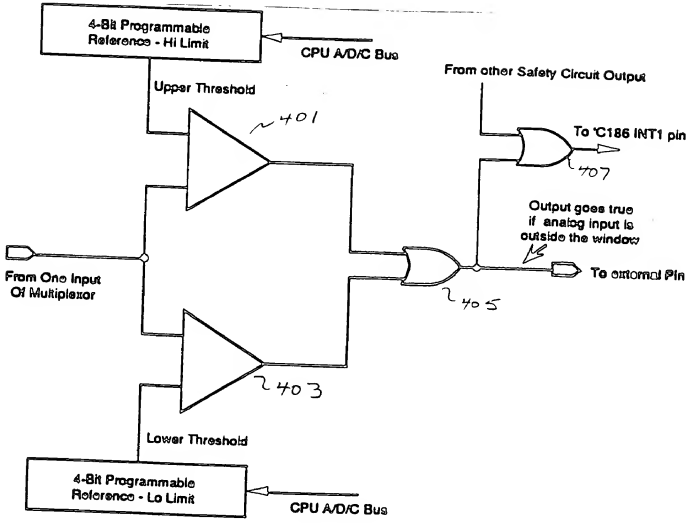
4-Bit Programmable
Reference - Hi Limit
CPU A/D/C Bus
Upper Threshold
401
From other Safety Circuit Output
To 'C186 INT1 pin
407
Output goes true
if analog input is
outside the window
To external Pin
From One Input
Of Multiplexer
405
403
Lower Threshold
4-Bit Programmable
Reference - Lo Limit
CPU A/D/C Bus

FIGURE 4

Resolution	8 bits
Digital Code	Unipolar, magnitude only

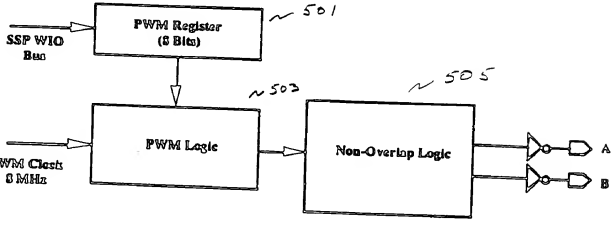

FIGURE 5a

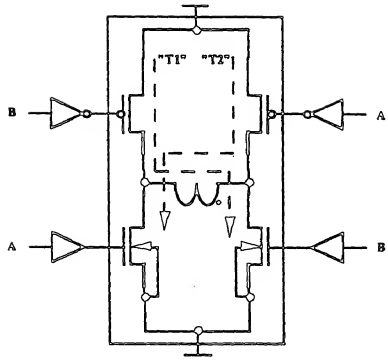

Figure 5b Typical Driver Connected to PWM Output

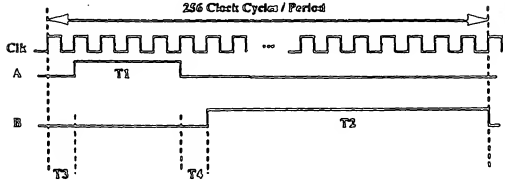

Figure 5c Pulse-Width Modulation Timing

Notes:
1 cycle = 125ns
1 cycle ≤ T1 ≤ 253 cycles
T3 = T4 = 1 cycle (Non-Overlap Delay Time)
T2 = (256 - 2 - T1) cycles

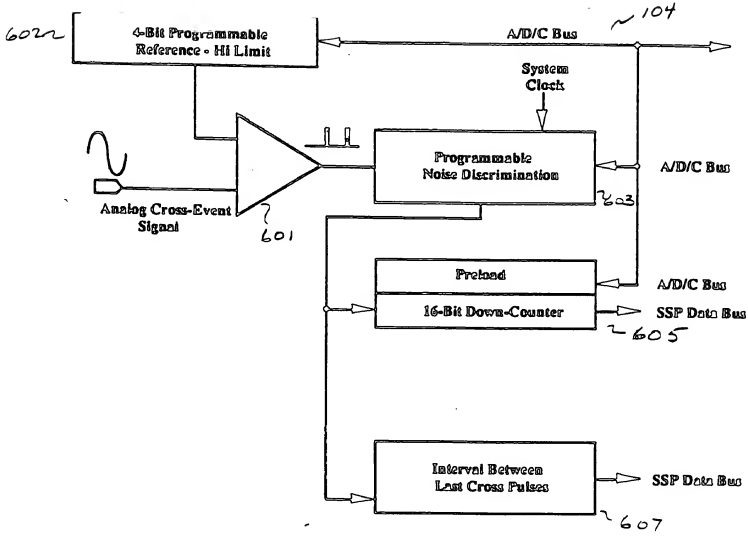
602
4-Bit Programmable
Reference - Hi Limit
104
A/D/C Bus
System
Clock
Programmable
Noise Discrimination
A/D/C Bus
603
Analog Cross-Event
Signal
601
Preload
A/D/C Bus
16-Bit Down-Counter
SSP Data Bus
605
Interval Between
Last Cross Pulses
SSP Data Bus
607

FIGURE 6